



## INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

### Verilog Implementation, Synthesis & Physical Design of MOD 16 Counter

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#### Abstract

In this paper, MOD 16 up counter has been implemented using Cadence front end tools. Verilog RTL has been used for writing the code of counter. The functionality of counter has been tested by writing the testbench of counter and observing its output waveform. Synthesized circuit and gate level netlist is generated by the synthesis tool. It also gives area, power and timing report which is satisfactory for the current design. Finally, physical design of counter is done which includes stages like floorplanning, power planning, placement, clock tree synthesis and routing. Setup time and hold time violations have been checked after routing stage. Total negative slack and worst negative slack have been found to be zero. Total power dissipation is 11767.597 nW and total area occupied by 13 cells of synthesized circuit is 88.200 units.

**Keywords:** Counter, Synthesis, Physical Design, RTL, MOD 16, Netlist

#### Introduction

A counter is a logic circuit that counts the number of occurrence of an input. Each count is called the state of the counter. The number of different states of the counter is known as modulus of the counter [3].

There are many applications of counter in electronics. Counters are widely used in almost all digital circuits such as measuring systems, analogue to digital converters, and various arithmetic operations [1]. Other applications are: frequency divider in phase-locked loops, frequency synthesizers, signal generation and processing circuits, microcontrollers, digital memories and in digital clock and timing circuits [4].

The table for 4 bit binary counter is shown in table 1. Q3 is MSB of counter and Q0 is LSB of counter. The counter increments its value after every positive edge of the clock. After 15<sup>th</sup> clock pulse, the counter reaches its maximum value 1111 and resets to 0000 after next clock pulse.

The 4-bit up counter is implemented using Cadence EDA tool [5]. The tool provides softwares for front end design such as Incisive tool for RTL code simulation and debugging, Encounter RTL Complier for synthesis and netlist generation, and Cadence Encounter tool for physical design – floorplanning, placement and routing.

Synchronous counter is generally used in most of the applications. In these counters, common clock is applied to all the flip flops which changes state at same time. On the other hand, in asynchronous counters, output of one flip flop drives clock input of other flip flop such that positive trigger is achieved when output of preceeding flip flop changes from low to high.

*Table 1. Bit Binary Counter*

Clock Pulse	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

### RTL testbench

Verilog testbench verifies the functionality of MOD 16 counter. It also helps in identifying the bugs if any in RTL code. A clock pulse of 10ns is generated in the testbench which increments the counter. Reset signal is also generated in the testbench, which is kept high in the beginning and makes transition to LOW level after 20 ns.

Counter module is instantiated in the testbench and name of counter instance is z1. It receives the clock pulse and reset signal from the testbench and generates output q which is incremented after every clock pulse. RTL testbench is shown below:

```

module test_counter();
reg clk=1'b0;
reg rst;
wire [3:0] q;

counter c1(clk,rst,q);

always #5 clk=~clk;

initial
begin
rst=1'b1;
#40 rst=1'b0;
end

initial
begin
#800 $finish;
end
endmodule

```

Counter constraints have been set in order to avoid clock slew situation and to define clock swing range. Constraints are declared as shown below:

```

create_clock -name clk -period 6 -waveform {0 3}
[get_ports "clk"]

```

The constraint ensures that clock period is atleast 6 ns to avoid setup time and hold time violations. It also sets clock swing range between 0 to 3V.

Simulation is performed using Cadence Incisive Simulation software. Snapshot of simulation window

is shown in figure 1. The counter output q increments after every clock pulse. It increments from decimal 0 to decimal 15 and then resets to decimal 0 after next clock pulse.



*Fig -1: Simulation Results*

### Synthesis

Synthesis is performed by Cadence Encounter RTL Compiler tool. The synthesized circuit is shown in figure 2. There are 13 cells in the synthesized circuit consisting of 4 DFF, 1 NAND gate, 5 NOR gates, 2 XNOR gates and 1 XOR gate.

Circuit has 2 inputs – reset and clock and one output q which I incremented after every positive edge of clock. Reset signal goes to all 4 positive edge triggered D flip flop's.

### Netlist Generated

Encounter RTL Compiler tool also generates gate level netlist from the RTL code. Netlist generated is structural style Verilog code in which output of one gate is connected to input of other gate. The netlist is shown in figure 3. Corresponding circuit performs the same functionality as was intended in RTL code.

### Area & Power Dissipation

The area report gives the area occupied by each of 13 cells which is shown in table 2. There are 4 instances of D flip flops which consume maximum area of 53.626 units. NAND gate occupies minimum area of 2.822 units. Total area occupied is 88.200 units.

The power dissipation of complete design – leakage power, dynamic power and total power is shown in table 3. Leakage power is very less as compared to

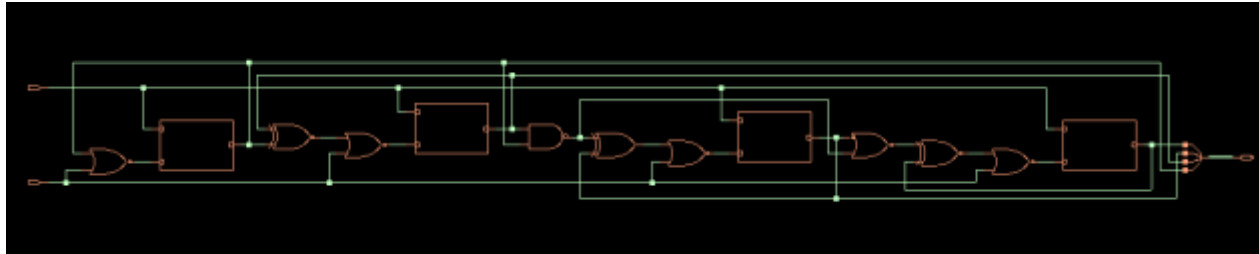


Fig -2: Circuit

dynamic power dissipation which is more than 95% of total power dissipation.

Fanout is driving capability of cell and slew is measure of how fast the output responds to change in input.

```
// Generated by Cadence Encounter(R) RTL Compiler v11.10-p005_
// Verification Directory fv/counter
module counter(clk, rst, q);
input clk, rst;
output [3:0] q;
wire clk, rst;
wire [3:0] q;
wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
wire n_8;
DFFQXL \q_reg[3] (.CK (clk), .D (n_8), .Q (q[3]));
NOR2X1 g63(.A (n_7), .B (rst), .Y (n_8));
DFFQXL \q_reg[2] (.CK (clk), .D (n_6), .Q (q[2]));
XNOR2X1 g65(.A (n_3), .B (q[3]), .Y (n_7));
DFFQXL \q_reg[1] (.CK (clk), .D (n_4), .Q (q[1]));
NOR2X1 g66(.A (n_5), .B (rst), .Y (n_6));
XOR2X1 g68(.A (n_2), .B (q[2]), .Y (n_5));
NOR2X2 g70(.A (n_1), .B (rst), .Y (n_4));
DFFQXL \q_reg[0] (.CK (clk), .D (n_0), .Q (q[0]));
NOR2BX1 g69(.AN (q[2]), .B (n_2), .Y (n_3));
XNOR2X1 g72(.A (q[1]), .B (q[0]), .Y (n_1));
CLKNAND2X2 g73(.A (q[1]), .B (q[0]), .Y (n_2));
NOR2X1 g74(.A (q[0]), .B (rst), .Y (n_0));
endmodule
```

Fig -3: Netlist Generated

Table 2. Area Occupied

Gate	Instances	Area
NAND Gate	1	2.822
D Flip Flop	4	53.626
NOR Gate	5	14.817
XNOR Gate	2	11.290
XOR Gate	1	5.645
TOTAL	13	88.200

**Timing Analysis**

The timing report is shown in table 4.

It provides the following information:

- Type of cell
- Fanout, load, slew, and total cell delay
- Arrival time

Table 3. Power Dissipation

Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)
284.021	11483.576	11767.597

Table 4. Timing Report

Type	Fanout	Load (ff)	Slew (ps)	Delay (ps)	Arrival (ps)
D Flip Flop	4	5.3	123	245	245
NAND Gate	2	3.4	58	58	303
NOR Gate	1	1.8	45	39	342
XNOR Gate	1	1.7	75	71	412

**Physical design**

Cadence Encounter RTL Compiler has been used for physical design.

The different stages in physical design flow are:

- Floorplanning
- Power Planning
- Placement
- Clock-tree Synthesis (CTS)
- Routing

The first step in the physical design flow is Floorplanning. In floorplanning, the core chip area is allocated. This is the area in which whole core circuitry is placed. It decided the boundary of the core.

In the current design, specifications for floorplanning are:

- Core to Left = 5 um
- Core to Right = 5 um
- Core to Top = 5um
- Core to Bottom = 5um

The resultant output is shown in figure 4, where distance from core to I/O boundary is 5um.

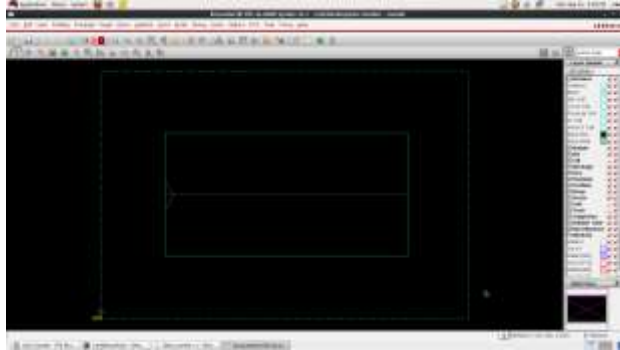


Fig -4: Floorplanning Output

Next stage is power planning in which VDD and VSS are selected. Specifications chosen are:

Metal Layer in Top & Bottom = Metal 5  
 Metal Layer in Left & Right = Metal 6

Rings and stripes are added in the design as shown in figure 5.

After power planning, next stage is placement in which exact position of a block is decided. Different placement algorithms are used for that which considers various parameters. Some of these parameters are wire length, delay, timing constraints etc. Blocks which communicate with each other very frequently are placed close to each other.

Clock tree synthesis minimizes clock skew and if necessary inserts clock buffer. Generally, clock is distributed using H tree path so that clock source to all destinations distance is equal.

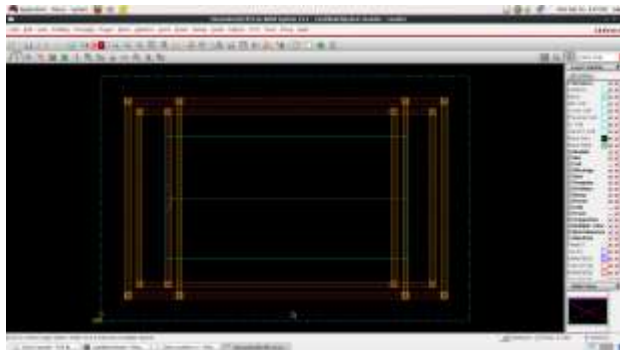


Fig -5: Power planning Output

Routing connects different blocks using different metal layers which can go upto 9 or 10 layers. Vias are also used while routing different metal layers over same point. Layout after routing stage is shown in figure 6.

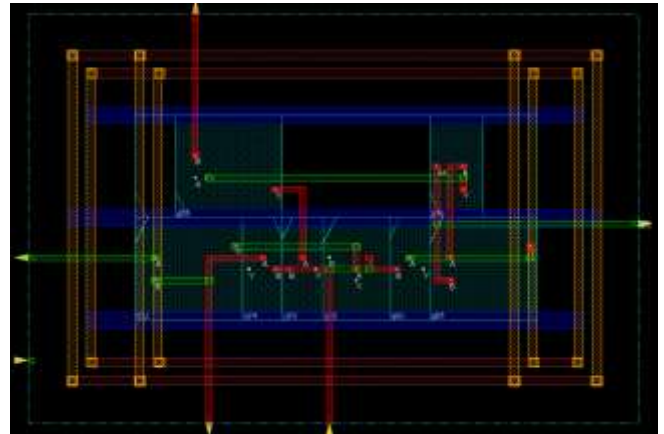


Fig -6: Layout

**Timing Report after routing**

After routing, set up time and hold time violations are checked in the design. In current design, no slack has been as shown in figure 7 below.

WNS is worst negative slack and TNS is total negative slack. Negative slack implies that delay in that path is high and signal should arrive early.

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 timeDesign Summary  
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Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.000	N/A	N/A	N/A	N/A	N/A
TNS (ns):	0.000	N/A	N/A	N/A	N/A	N/A
Violating Paths:	0	N/A	N/A	N/A	N/A	N/A
All Paths:	0	N/A	N/A	N/A	N/A	N/A

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)

Density: 70.000%  
 Routing Overflow: 0.00% H and 0.00% V

Fig -7: Timing Analysis

**Conclusion**

Counter is very important block in VLSI. Counter is the widest application of flip - flops. A counter is one of the more useful digital circuits [2]. Counter counts the number of occurrences of an events for controlling certain processes [6]. Some of the applications of counter are frequency synthesizers, signal generation and processing circuits,

microcontrollers, digital memories, measuring systems, analogue to digital converters, and various arithmetic operations etc.

In this work, MOD 16 up counter has been implemented using Cadence Incisive tool for RTL code simulation and debugging, Encounter RTL Complier for synthesis and netlist generation, and Cadence Encounter tool for physical design – floorplanning, placement and routing.

Verilog testbench verifies the functionality of RTL code and synthesized circuit is generated along with area, power and timing report. The RTL code can be modified to optimize area, power and timing results. In current design, area, power and timing reports are satisfactory.

Finally, physical design – floorplanning, placement, routing is done and slacks are checked for any setup or hold time violations. The MOD 16 counter is optimum in terms of area, power and timing analysis.



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### Author Bibliography

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